

Notice of References Cited	Application/Control No. 10/078,876	Applicant(s)/Patent Under Reexamination HATHAWAY ET AL.	
	Examiner Joseph D. Torres	Art Unit 2133	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-6,529,861	03-2003	Patra et al.	703/14
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
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	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	J. Monteiro, S. Devadas, and B. Lin, "A Methodology for Efficient Estimation of Switching Activity in Sequential Logic Circuits," Proc. 31st Design Automation Conf., pp. 12-17, 1994
	V	Seiji Kajihara, Kohei Miyase: On Identifying Don't Care Inputs of Test Patterns for Combinational Circuits. ICCAD 2001: 364-369
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*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.